Official Amendment
Serial No. 09/943,078
Docket No. MIO 0083 PA/40509.162

Remarks

Claims 50-58 are currently pending, all were rejected in the Office Action of April 12, 2005. Claims 50 and 58 have been amended and claims 53 and 54 have been withdrawn.

Rejections Under 35 U.S.C. § 112

Claims 50-58 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Applicant respectfully traverses.

Support for the subject matter of the limitation that the lightly-doped drain regions and source/drain regions are "adjacent and lateral" to the local interconnect structure can be found in the Specification on page 12, lines 10-24, and in the figures 12A-12B and 13 (elements 94-96) as originally filed. The spacers are formed against the vertical walls of the damascene local interconnect structure (page 12, lines 11-12) and the doped regions are formed adjacent to the LDD region that is underneath the spacer (page 12, lines 21-23). The lightly-doped drain region and the doped regions jointly define the doped source/drain regions (page 12, lines 23-24). Therefore, the lightly-doped drain regions and source/drain regions are adjacent the local interconnect structure. The word "lateral" is not specifically used in the Specification. However, the Merriam-Webster dictionary defines "lateral" to mean "of or relating to the side." The lightly-doped drain regions 94 and source/drain regions 96 are clearly illustrated in Figs 12A-12B and 13 to be adjacent and lateral to the local interconnect structure 70.

Therefore, Applicant believes claims 50-58 do comply with the written description requirement and requests that the Examiner withdraw his rejection to claims 50-58

Claim 58 was rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

the Applicant regards as the invention.

Accordingly, claim 58 was amended to remove the phrase "said damascene local interconnect structure" from lines 15-16 in the claim. Further, claim 58 was amended to clarify the phrase "forming doped source/drain regions in said base substrate after forming said spacers such that said base substrate is doped more deeply into said base substrate adjacent and lateral to said spacers than into said base substrate underneath said spacers" to read "forming doped regions in said base substrate after formation of said spacers such that said base substrate is doped more deeply adjacent and lateral to said spacers and said lightly doped drain regions underneath said spacers, wherein said lightly doped drain regions and said doped regions define doped source/drain regions." Support for this amendment can be found on page 12, lines 19-24, of the Specification

Applicant believes that claim 58 is now in compliance with 35 U.S.C. § 112, second paragraph and requests that the Examiner withdraw his rejection to claim 58.

Rejections Under 35 U.S.C. § 102(b)

Claims 50-52 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lin. Applicant respectfully traverses this rejection.

Claim 50, as amended, recites a method of fabricating a semiconductor device by forming a damascene trench in a first dielectric layer over a base substrate. The damascene trench has both a gate area and a local interconnect area. A conductive layer is deposited over the base substrate such that the damascene trench is filled with a conductive material. The device is planed to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by the conductive material within the damascene trench. The damascene local interconnect structure forms a direct connection to the base substrate. At least one implant contact is provided within a plug area. The plug area is located at least partially

beneath and in contact with the damascene local interconnect structure. Spacers are shaped against the vertical walls of the damascene gate structure and the damascene interconnect structure. Doped source/drain regions are formed in the base substrate adjacent and lateral to the damascene gate structure and the damascene local interconnect structure.

Lin disclose a method for simultaneously fabricating a gate conductive layer and a local interconnect. However, Lin fails to disclose shaping spacers on the vertical walls of the local interconnect structure. Instead, Lin discloses forming spacers on the vertical walls of the gates and then removing one spacer and the dielectric layer on one side of a gate in order to form the local interconnect opening (Col. 3, lines 8-12). In contrast, in the claimed invention, the sidewalls are formed on both sides of the local interconnect structure after formation of the local interconnect structure. Further, in Lin, the local interconnect is formed over the exposed source/drain region (Col. 3, lines 10-12) as opposed to forming the local interconnect over a plug area as disclosed in the claimed invention. Therefore, Applicant believes that claim 50 is not anticipated by Lin and requests the Examiner withdraw his rejection to claim 50.

Claims 51 and 52 depend on independent claim 50 either directly or ultimately. These dependent claims are patentable for the same reasons as presented above with respect to the claim from which they depend. Consequently, the Applicant believes this rejection also is unsupported by the cited references and requests that the Examiner withdraw his rejections to these claims.

Rejections Under 35 U.S.C. § 103(a)

Claim 58 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsutsumi in view of the basic text of Ghandi. Applicant respectfully traverses this rejection.

Independent claim 58 recites, in part, a method for fabricating a semiconductor

device. A damascene trench is formed in a first dielectric layer of the base substrate. The damascene trench has both a gate area and a local interconnect area. At least one implant contact is provided within a plug area. The plug area is located at least partially beneath and in contact with the damascene local interconnect structure. Conductive material is deposited over the base substrate to fill the damascene trench. The device is then planed to define a damascene structure with a damascene gate structure and a damascene local interconnect structure. A direct connection is made between the damascene local interconnect structure and the base substrate. Doped source/drain regions are formed within the base substrate adjacent and lateral to the damascene gate structure and a damascene local interconnect structure.

Tsutsumi fails to disclose forming the source/drain regions adjacent and lateral to the damascene local interconnect structure. Instead, Tsutsumi discloses forming the source/drain regions 11 and 13 directly beneath the paired source/drain electrodes 14 (Col. 12, lines 37-45; Figs. 10-14) which forms the connection to the interconnection 16. The source/drain regions 11 and 13 are not adjacent and lateral to the damascene local interconnect structure as disclosed in the claimed invention and discussed above. In the claimed invention, the local interconnect area is formed over a plug area not a doped source/drain region.

Ghandi does not remedy the deficiencies of Tsutsumi. Ghandi also fails to suggest or teach source/drain regions adjacent and lateral to the damascene local interconnect structure. Nor does the hypothetical combination of Tsutsumi and Ghandi suggest or teach source/drain regions adjacent and lateral to the damascene local interconnect structure. Because the hypothetical combination of Tsutsumi and Ghandi does not suggest or teach all the features of the claimed invention, Applicant believes that claim 58 is patentable over the prior art and requests the Examiner withdraw his rejection to claim 58.

Claim 55-57 was rejected under 35 U.S.C. § 103(a) as being unpatentable over

Tsutsumi in view of Lin. Applicant respectfully traverses this rejection.

Claim 55 recites a method of fabricating a semiconductor device by forming a damascene trench in a first dielectric layer over a base substrate. The damascene trench has a gate area and a local interconnect area. A conductive layer is deposited over said base substrate such that the damascene trench is filled with a conductive material. The conductive material comprises a polysilicon material. The device is planed to define a damascene structure including a damascene gate structure and a damascene local interconnect structure electrically coupled by the conductive material within the damascene trench. The damascene local interconnect structure forms a direct connection to the base substrate. A silicide layer is formed over the polysilicon material within the gate area of the damascene trench. Doped source/drain regions are formed in the base substrate adjacent and lateral to the damascene gate structure and the damascene local interconnect structure.

As discussed above, Tsutsumi fails to disclose forming the source/drain regions adjacent and lateral to the damascene local interconnect structure. Instead, Tsutsumi discloses forming the source/drain regions 11 and 13 directly beneath the paired source/drain electrodes 14 (Col. 12, lines 37-45; Figs. 10-14) which forms the connection to the interconnection 16. The source/drain regions 11 and 13 are not adjacent and lateral to the damascene local interconnect structure as disclosed in the claimed invention and discussed above. In contrast, in the claimed invention, the local interconnect is formed on top of the plug area.

Examiner admits Tsutsumi fails to teach that the local interconnect structure and the gate structure are electrically coupled by the conductive material in the damascene trench and cites Lin. However, Lin fails to remedy the deficiencies of Tsutsumi. As discussed above, Lin discloses a method for simultaneously fabricating a gate conductive layer and a local interconnect. However, Lin also fails to disclose doped source/drain regions formed in the base substrate adjacent and lateral to the damascene local interconnect structure. Instead, Lin discloses forming the local

interconnect in a space formed on top of a source/drain region of a gate and the sidewall of a gate (Col. 2, lines 14-16; Col. 3, lines 8-12). Thus, the local interconnect is formed on top of this source/drain region and over the gate.

Neither Tsutsumi nor Lin disclose doped source/drain regions formed in the base substrate adjacent and lateral to the damascene local interconnect structure. Therefore, neither Tsutsumi nor Lin disclose these features of the claimed invention.

Nor does the hypothetical combination of Tsutsumi and Lin suggest or teach doped source/drain regions formed in the base substrate adjacent and lateral to the damascene local interconnect structure. At best, the hypothetical combination teaches forming a local interconnect over the source/drain region that is electrically coupled to a gate structure. Because the hypothetical combination of Tsutsumi and Lin does not suggest or teach all the features of the claimed invention, Applicant believes that claim 55 is patentable over the prior art and requests the Examiner withdraw his rejection to claim 55.

Independent claim 56, as amended, also recites doped source/drain regions formed in the base substrate adjacent and lateral to the damascene gate structure and the damascene local interconnect structure as is called for in claim 55. Therefore, for the same reasons discussed above, Applicant believes claim 56 is also patentable over the cited references, and requests that the Examiner withdraw his rejection of claim 56.

Claim 57 depends on independent claim 56. This dependent claim is patentable for the same reasons as presented above with respect to the claim from which it depends. Consequently, the Applicant believes this rejection also is unsupported by the cited references and requests that the Examiner withdraw his rejections to this claim.

CONCLUSION

Applicant respectfully submits that the above claims represent allowable subject matter. The Examiner is encouraged to contact the undersigned to resolve efficiently any formal matters or to discuss any aspects of the application or of this response. Otherwise, early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,
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